This Page is Inserted by IFW Indexing and Scanning Operations and is not part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

☐ BLACK BORDERS
☐ IMAGE CUT OFF AT TOP, BOTTOM OR SIDES
☐ FADED TEXT OR DRAWING
☐ BLURRED OR ILLEGIBLE TEXT OR DRAWING
☐ SKEWED/SLANTED IMAGES
☐ COLOR OR BLACK AND WHITE PHOTOGRAPHS
☐ GRAY SCALE DOCUMENTS
☐ LINES OR MARKS ON ORIGINAL DOCUMENT
☐ REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY

IMAGES ARE BEST AVAILABLE COPY.

As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.



United States Patent and Trademark Office

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

FIRST NAMED INVENTOR ATTORNEY DOCKET NO. APPLICATION NO. FILING DATE CONFIRMATION NO. Eric John Hewitt AHA-02101 09/808,884 03/14/2001 **EXAMINER** 28960 09/07/2004 TORRES, JOSEPH D HAVERSTOCK & OWENS LLP 162 NORTH WOLFE ROAD PAPER NUMBER ART UNIT SUNNYVALE, CA 94086

2133

DATE MAILED: 09/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)	
	09/808,884	HEWITT ET AL.	
Office Action Summary	Examiner	Art Unit	
	Joseph D. Torres	2133	
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply			
A SHORTENED-STATUTORY PERIOD FOR REPLY-IS-SET-TO-EXPIRE-3 MONTH(S)-FROM— THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).			
Status			
1) Responsive to communication(s) filed on 14 March 2001.			
2a) This action is FINAL . 2b) This action is non-final.			
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.			
Disposition of Claims			
4) Claim(s) 1-40 is/are pending in the application. 4a) Of the above claim(s) 8-10 is/are withdrawn from consideration. 5) Claim(s) is/are allowed. 6) Claim(s) 1-7 and 11-40 is/are rejected. 7) Claim(s) is/are objected to. 8) Claim(s) are subject to restriction and/or election requirement.			
Application Papers			
9) The specification is objected to by the Examiner.			
10)⊠ The drawing(s) filed on <u>14 March 2001</u> is/are: a)□ accepted or b)⊠ objected to by the Examiner.			
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).			
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.			
Priority under 35 U.S.C. § 119			
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 			
Attachment(s)			
1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) Paper No(s)/Mail Date			
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 5) Notice of Informal Patent Application (PTO-152) Other:			

Art Unit: 2133

DETAILED ACTION

Election/Restrictions

- 1. Restriction to one of the following inventions is required under 35 U.S.C. 121:
 - Claims 1-7 and 11-40, drawn to serially concatenated codes, classified in class 714, subclass 755.
 - II. Claims 8-10, drawn to a method for rotating sub-blocks for generating a hyper-code, classified in class 714, subclass 752.

The inventions are distinct, each from the other because of the following reasons: Inventions Group I and Group II are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because generating a hyper-code does not require a means for rotting sub-blocks. The subcombination has separate utility such as in serially concatenated encoders.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Art Unit: 2133

Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group II is not required for Group I, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

During a telephone conversation with Thomas Haverstock on 23 August 2004 a provisional election was made without traverse to prosecute the invention of Group I, claims 1-7 and 11-40. Affirmation of this election must be made by applicant in replying to this Office action. Claims 8-10 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in

Art Unit: 2133

the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Oath/Declaration

2. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because: It does not have a dated signature for each inventor.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 4, 5, 11-22, 30-35 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. Claim 4 recites, "the step of initializing the parity array such that the parity bits are set to zero before the step of performing the parity calculation along the hyper diagonal is executed". The omitted structural cooperative relationships are: the relationship explaining "initializing the parity array" ... "before the step of performing the parity calculation along the hyper diagonal is executed" since the

Art Unit: 2133

parity array is generated in claim 2 as a result of the parity calculation in and did not exist prior to that according to the claim language.

Claim 5 recites the limitation "the encoded block" in lines 1 and 2. There is insufficient antecedent basis for this limitation in the claim.

Claim 11 recites, "receiving a row of the block and immediately outputting the row" in lines 4. The term "immediately" in claim 4 is a relative term which renders the claim indefinite. The term "immediately" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. Note: there is no structural element in the language "receiving a row of the block and immediately outputting the row" by which one of ordinary skill in the art at the time the invention was made would have been able to ascertain what is meant by "immediately".

Claim 11 recites the limitation "the updated second set" in line 15. There is insufficient antecedent basis for this limitation in the claim.

Claims 12 and 13 are incomprehensible. It is not clear whether the applicant is attempting to claim an alternative embodiment of claim 11 or whether the Applicant is claiming additional encoding schemes to supplement the three encoding devices in claim 11.

Art Unit: 2133

Claim 18 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. Claim 18 recites, "resetting the row encode storage array such that all row array bits are set to zero, wherein the step of resetting is executed after the first set of encoded data is outputted". The omitted structural cooperative relationships are: the relationship between "resetting the row encode storage array", the "storage array" and the encoding steps of claim 11.

The term "predetermined number of bits" in claim 21 is a relative term which renders the claim indefinite. The term "predetermined number of bits" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. It is unclear what the Applicant means by rotating. Rotating is a geometric operation and it is unclear how rotating an abstraction used to explain the operation of an encoder has anything to do with any structural component et within the encoder.

Claim 30 recites the limitation "the encoded bits" in line 14. There is insufficient antecedent basis for this limitation in the claim. "The encoded bits" could refer to either "encoded row bits" or "encoded column bits". The Examiner assumes the applicant intended: "encoded column bits".

Art Unit: 2133

Claim 38 recites the limitation "each diagonal encoded" in lines 3-4. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 4. Claims 1-3, 5-7, 23-29, 37 and 38 are rejected under 35 U.S.C. 102(b) as being anticipated by Rhines; Don S. et al. (US 5392299 A, hereafter referred to as Rhines).

35 U.S.C. 102(b) rejection of claims 1.

Rhines teaches performing a parity calculation along a hyper diagonal in the block, wherein a parity result for the parity calculation is generated (col. 4, lines 59-62 and col. 10, lines 31-68 in Rhines teach that prior to generating the C2 error correction 90 of Figure 2 in Rhines, the rows of the first series of data planes 40, 42 and 44 in Figures 4A and 5 are orthogonally shuffled by the outer Interleaver 16 so that the new block of Figure 4B is formed whereby the x-y planes of the new block of Figure 4B are the diagonal planes of the Block in Figure 4A; hence the column encoding of the new block of Figure 4B to from the C2 error correction of Figures 2 and 8 is equivalent and is a means for performing a parity calculation along a hyper diagonal in the Block in Figure

Art Unit: 2133

4A, wherein a parity result for the C2 parity calculation of Figure 8 is generated); and adding the parity result to the block of data (Figure 8 in Rhines teaches adding the C2 parity result to the block of data).

35 U.S.C. 102(b) rejection of claim 2.

Rhines teaches that the C2 parity is a separate array from the User Data array added to the User Data array in Figure 8.

35 U.S.C. 102(b) rejection of claim 3.

The shuffling steps of Figures 4A, 4B and 5 in Rhines are a means for rotating the parity array for calculating C2 parity such that the C2 parity result stored in the C2 parity array is substantially aligned with the hyper diagonal planes in Figure 4B along which the C2 parity result was calculated.

35 U.S.C. 102(b) rejection of claim 5.

The shuffling steps of Figures 4A, 4B and 5 in Rhines are a means for rotating the parity array for calculating C2 parity such that the C2 parity result stored in the C2 parity array is substantially aligned with the hyper diagonal planes in Figure 4B along which the C2 parity result was calculated. Note: the C2 encoded block of data is outputted from Middle Ecnoder 90 when the parity result is aligned substantially with the hyper diagonal and after the C2 parity is calculated.

Art Unit: 2133

35 U.S.C. 102(b) rejection of claim 6.

Figures 4A, 4B and 5 in Rhines teach that the block of data is three-dimensional.

35 U.S.C. 102(b) rejection of claim 7.

Rhines teaches that the C2 parity is a separate 3-d hyper-plane from the User Data 3-d block added to the User Data array in Figure 8.

35 U.S.C. 102(b) rejection of claim 23.

Rhines teaches a datapath module for encoding a block of data having a plurality of systematic block code codewords (Middle Encoder 100 in Figure 2 of Rhines is a datapath module for encoding a block of data having a plurality of systematic block code codewords), wherein each codeword includes a plurality of information bits and a plurality of error correction bits (see Figure 3 in Rhines), wherein the datapath module hyper-diagonally encodes a string of the block code codewords and performs a parity calculation on the string, whereby a parity result for each string is generated (col. 4, lines 59-62 and col. 10, lines 31-68 in Rhines teach that prior to generating the C2 error correction 90 of Figure 2 in Rhines, the rows of the first series of data planes 40, 42 and 44 in Figures 4A and 5 are orthogonally shuffled by the outer Interleaver 16 so that the new block of Figure 4B is formed whereby the x-y planes of the new block of Figure 4B are the diagonal planes of the Block in Figure 4A; hence the column encoding of the new block of Figure 4B to from the C2 error correction of Figures 2 and 8 is equivalent

Art Unit: 2133

and is a means for performing a parity calculation along a hyper diagonal in the Block in Figure 4A, wherein a parity result for the C2 parity calculation of Figure 8 is generated).

35 U.S.C. 102(b) rejection of claim 24.

Figure 13A is a parity array for storing parity results.

35 U.S.C. 102(b) rejection of claim 25.

Outer Interleaver 16 in Rhines is an input module for receiving the block of data.

35 U.S.C. 102(b) rejection of claim 26.

Media Channel Encoder 160 in Rhines is an output module for outputting the block of encoded data.

35 U.S.C. 102(b) rejection of claim 27.

Rhines teaches receiving a column of the block and immediately outputting the columns (Figure 2 and 3 of Rhines teach receiving a stream outputted form a source data as columns to the Outer C3 column encoder 16 in Figure 2); encoding the information bits in the column, wherein a first set of encoded data is generated according to a first encoding scheme and outputting the first set of encoded data (the Outer C3 column encoder 16 in Figure 2 of Rhines is a means for encoding the information bits in the column, wherein a first set of encoded data is generated according to a first encoding scheme and outputting the first set of encoded data in Figure 3 of Rhines); encoding the

Art Unit: 2133

information bits in a rows according to a second encoding scheme, wherein a second set of encoded data is generated and iteratively updated according to the information bits in the columns (the Inner C1 row encoder 150 in Figure 2 of Rhines is a means for encoding the user data information bits in Figure 13A in Rhines in a rows according to a second C1 encoding scheme, wherein a second set of encoded data is generated and iteratively updated according to the information bits in the columns; Note: the C1 encoder must iteratively receive user data information bits in rows since Inner C1 row encoder 150 in Figure 2 is a row encoder); e. hyper-diagonally encoding the information bits in the block according to a parity encoding scheme, wherein a hyper set of encoded data is generated according to the information bits in the row and column and the first (col. 4, lines 59-62 and col. 10, lines 31-68 in Rhines teach that prior to generating the C2 error correction 90 of Figure 2 in Rhines, the rows of the first series of data planes 40, 42 and 44 in Figures 4A and 5 are orthogonally shuffled by the outer Interleaver 16 so that the new block of Figure 4B is formed whereby the x-y planes of the new block of Figure 4B are the diagonal planes of the Block in Figure 4A; hence the column encoding of the new block of Figure 4B to from the C2 error correction of Figures 2 and 8 is equivalent and is a means for performing a parity calculation along a hyper diagonal in the Block in Figure 4A, wherein a parity result for the C2 parity calculation of Figure 8 is generated; Note: the Middle C2 encoder must iteratively receive user data information bits in hyper columns since Middle C2 hyper column encoder 90 in Figure 2 is a hyper column encoder); outputting the updated set of encoded data after all the information bits and all subsequent first sets of encoded data are outputted (Inner C1 row encoder

Art Unit: 2133

after all the information bits and all subsequent first sets of encoded data are outputted); and outputting the hyper set of encoded data (C2 error encoder 90 of Figure 2 in Rhines is a means for outputting the hyper set of encoded data). Note: because of the symmetry of a 3-d block of data interchanging the rows with columns so that the first encoder in Rhines is a row encoder and the third encoder is a column encoder with the second encoder being a hyper encoder does not change the teachings of Rhines and such an encoding device is inherently equivalent to the encoder in Rhines.

However Rhines does not explicitly teach the specific use of hyper set of encoded data generated based on second sets of encoded data, that is, an arrangement whereby the first encoder in a set of serially concatenated encoders is a row encoder, the second encoder is a column encoder and the third encoder is a hyper encoder.

35 U.S.C. 102(b) rejection of claim 28.

Multiplexers 70 and 80 in Figure 6 are coupled to all the encoder modules for outputting the encoded block of data.

35 U.S.C. 102(b) rejection of claim 29.

Hyper encoding is a third encoding scheme; hence C2 error correction 90 of Figure 2 in Rhines is a third encoding module for encoding a plurality of planes from the block of data, wherein the third encoder adds the error correction bits to the planes.

Art Unit: 2133

35 U.S.C. 102(b) rejection of claims 37 and 38.

Rhines teaches receiving a column of the block and immediately outputting the columns (Figure 2 and 3 of Rhines teach receiving a stream outputted form a source data as columns to the Outer C3 column encoder 16 in Figure 2); encoding the information bits in the column, wherein a first set of encoded data is generated according to a first encoding scheme and outputting the first set of encoded data (the Outer C3 column encoder 16 in Figure 2 of Rhines is a means for encoding the information bits in the column, wherein a first set of encoded data is generated according to a first encoding scheme and outputting the first set of encoded data in Figure 3 of Rhines); encoding the information bits in a rows according to a second encoding scheme, wherein a second set of encoded data is generated and iteratively updated according to the information bits in the columns (the Inner C1 row encoder 150 in Figure 2 of Rhines is a means for encoding the user data information bits in Figure 13A in Rhines in a rows according to a second C1 encoding scheme, wherein a second set of encoded data is generated and iteratively updated according to the information bits in the columns; Note: the C1 encoder must iteratively receive user data information bits in rows since Inner C1 row encoder 150 in Figure 2 is a row encoder); e. hyper-diagonally encoding the information bits in the block according to a parity encoding scheme, wherein a hyper set of encoded data is generated according to the information bits in the row and column and the first (col. 4, lines 59-62 and col. 10, lines 31-68 in Rhines teach that prior to generating the C2 error correction 90 of Figure 2 in Rhines, the rows of the first series of data planes 40, 42 and 44 in Figures 4A and 5 are orthogonally shuffled by the outer Interleaver 16

Art Unit: 2133

so that the new block of Figure 4B is formed whereby the x-y planes of the new block of Figure 4B are the diagonal planes of the Block in Figure 4A, hence the column encoding of the new block of Figure 4B to from the C2 error correction of Figures 2 and 8 is equivalent and is a means for performing a parity calculation along a hyper diagonal in the Block in Figure 4A, wherein a parity result for the C2 parity calculation of Figure 8 is generated; Note: the Middle C2 encoder must iteratively receive user data information bits in hyper columns since Middle C2 hyper column encoder 90 in Figure 2 is a hyper column encoder); outputting the updated set of encoded data after all the information bits and all subsequent first sets of encoded data are outputted (Inner C1 row encoder 150 in Figure 2 of Rhines is a means for outputting the updated set of encoded data after all the information bits and all subsequent first sets of encoded data are outputted); and outputting the hyper set of encoded data (C2 error encoder 90 of Figure 2 in Rhines is a means for outputting the hyper set of encoded data). Note: because of the symmetry of a 3-d block of data interchanging the rows with columns so that the first encoder in Rhines is a row encoder and the third encoder is a column encoder with the second encoder being a hyper encoder does not change the teachings of Rhines and such an encoding device is inherently equivalent to the encoder in Rhines. However Rhines does not explicitly teach the specific use of hyper set of encoded data generated based on second sets of encoded data, that is, an arrangement whereby the first encoder in a set of serially concatenated encoders is a row encoder, the second encoder is a column encoder and the third encoder is a hyper encoder.

Art Unit: 2133

35 U.S.C. 102(b) rejection of claim 39.

Rhines teaches that the C2 parity is a separate array from the User Data array added to the User Data array in Figure 8.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

- 1. Determining the scope and contents of the prior art.
- 2. Ascertaining the differences between the prior art and the claims at issue.
- 3. Resolving the level of ordinary skill in the pertinent art.
- 4. Considering objective evidence present in the application indicating obviousness or nonobviousness.
- 5. Claims 4, 11-22, 30-36 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rhines; Don S. et al. (US 5392299 A, hereafter referred to as Rhines).

35 U.S.C. 103(a) rejection of claim 4.

Rhines substantially teaches the claimed invention described in claims 1-3 (as rejected above).

Art Unit: 2133

However Rhines does not explicitly teach the specific use of initializing the parity array such that the parity bits are set to zero before the step of performing the parity calculation along the hyper diagonal is executed.

The Examiner asserts that the values of the C2 parity bits of Figures 4A, 4B and 5 in Rhines does not matter since any previous values would be discarded and replaced with newly calculated C2 parity bits because the current C2 parity bits only depend on the current calculation.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Rhines by including use of initializing the parity array such that the parity bits are set to zero before the step of performing the parity calculation along the hyper diagonal is executed. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of initializing the parity array such that the parity bits are set to zero before the step of performing the parity calculation along the hyper diagonal is executed would not have mattered since any previous values would be discarded and replaced with newly calculated C2 parity bits because the current C2 parity bits only depend on the current calculation.

35 U.S.C. 103(a) rejection of claims 11, 30, 32-36 and 40.

Rhines teaches receiving a column of the block and immediately outputting the columns (Figure 2 and 3 of Rhines teach receiving a stream outputted form a source data as columns to the Outer C3 column encoder 16 in Figure 2); encoding the information bits

Art Unit: 2133

in the column, wherein a first set of encoded data is generated according to a first encoding scheme and outputting the first set of encoded data (the Outer C3 column encoder 16 in Figure 2 of Rhines is a means for encoding the information bits in the column, wherein a first set of encoded data is generated according to a first encoding scheme and outputting the first set of encoded data in Figure 3 of Rhines); encoding the information bits in a rows according to a second encoding scheme, wherein a second set of encoded data is generated and iteratively updated according to the information bits in the columns (the Inner C1 row encoder 150 in Figure 2 of Rhines is a means for encoding the user data information bits in Figure 13A in Rhines in a rows according to a second C1 encoding scheme, wherein a second set of encoded data is generated and iteratively updated according to the information bits in the columns; Note: the C1 encoder must iteratively receive user data information bits in rows since Inner C1 row encoder 150 in Figure 2 is a row encoder); e. hyper-diagonally encoding the information bits in the block according to a parity encoding scheme, wherein a hyper set of encoded data is generated according to the information bits in the row and column and the first (col. 4, lines 59-62 and col. 10, lines 31-68 in Rhines teach that prior to generating the C2 error correction 90 of Figure 2 in Rhines, the rows of the first series of data planes 40, 42 and 44 in Figures 4A and 5 are orthogonally shuffled by the outer Interleaver 16 so that the new block of Figure 4B is formed whereby the x-y planes of the new block of Figure 4B are the diagonal planes of the Block in Figure 4A; hence the column encoding of the new block of Figure 4B to from the C2 error correction of Figures 2 and 8 is equivalent and is a means for performing a parity calculation along a hyper diagonal in

Art Unit: 2133

the Block in Figure 4A, wherein a parity result for the C2 parity calculation of Figure 8 is generated; Note: the Middle C2 encoder must iteratively receive user data information bits in hyper columns since Middle C2 hyper column encoder 90 in Figure 2 is a hyper column encoder); outputting the updated set of encoded data after all the information bits and all subsequent first sets of encoded data are outputted (Inner C1 row encoder 150 in Figure 2 of Rhines is a means for outputting the updated set of encoded data after all the information bits and all subsequent first sets of encoded data are outputted); and outputting the hyper set of encoded data (C2 error encoder 90 of Figure 2 in Rhines is a means for outputting the hyper set of encoded data). Note: because of the symmetry of a 3-d block of data interchanging the rows with columns so that the first encoder in Rhines is a row encoder and the third encoder is a column encoder with the second encoder being a hyper encoder does not change the teachings of Rhines and such an encoding device is inherently equivalent to the encoder in Rhines. However Rhines does not explicitly teach the specific use of hyper set of encoded data generated based on second sets of encoded data, that is, an arrangement whereby the first encoder in a set of serially concatenated encoders is a row encoder, the second encoder is a column encoder and the third encoder is a hyper encoder. The Examiner asserts that the triple orthogonal interleaved error correction system using a hyper diagonal encoder taught in Rhines is only an exemplary embodiment of triple orthogonal interleaved error correction systems and that rearranging the

exemplary embodiment of the triple orthogonal interleaved error correction system

taught in Rhines to produce an alternative embodiment whereby the first encoder in the

Art Unit: 2133

set of serially concatenated encoders is a row encoder, the second encoder is a column encoder and the third encoder is a hyper encoder is an obvious alternative embodiment as Rhines states in col. 25, col. 34-42 in Rhines since such a rearranged encoder is still a triple orthogonal interleaved error correction system.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Rhines by including use of hyper set of encoded data generated based on second sets of encoded data, that is, an arrangement whereby the first encoder in a set of serially concatenated encoders is a row encoder, the second encoder is a column encoder and the third encoder is a hyper encoder. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of hyper set of encoded data generated based on second sets of encoded data, that is, an arrangement whereby the first encoder in a set of serially concatenated encoders is a row encoder, the second encoder is a column encoder and the third encoder is a hyper encoder would have provided the opportunity to produce an alternative embodiment whereby the first encoder in the set of serially concatenated encoders is a row encoder, the second encoder is a column encoder and the third encoder is a hyper encoder is an obvious alternative embodiment as Rhines states in col. 25, col. 34-42 in Rhines since such a rearranged encoder is still a triple orthogonal interleaved error correction system.

35 U.S.C. 103(a) rejection of claims 12 and 13.

Art Unit: 2133

Claims 12 and 13 provide alternative embodiment for claim 11, in particular, using different coding schemes. The Examiner asserts that the triple orthogonal interleaved error correction system using a hyper diagonal encoder taught in Rhines is only an exemplary embodiment of triple orthogonal interleaved error correction systems and that rearranging the exemplary embodiment of the triple orthogonal interleaved error correction system taught in Rhines to produce an alternative embodiment whereby the first encoder in the set of serially concatenated encoders is a row encoder, the second encoder is a column encoder and the third encoder is a hyper encoder is an obvious alternative embodiment as Rhines states in col. 25, col. 34-42 in Rhines since such a rearranged encoder is still a triple orthogonal interleaved error correction system.

35 U.S.C. 103(a) rejection of claim 14.

Figures 4A, 4B and 5 in Rhines teach that the block of data is three-dimensional.

35 U.S.C. 103(a) rejection of claim 15.

Hyper encoding is a third encoding scheme; hence C2 error correction 90 of Figure 2 in Rhines is a third encoding scheme. Note: the Middle C2 encoder must iteratively receive user data information bits in hyper columns since Middle C2 hyper column encoder 90 in Figure 2 is a hyper column encoder

35 U.S.C. 103(a) rejection of claim 16.

Art Unit: 2133

Rhines teaches that the C2 parity is a separate 3-d hyper-plane from the User Data 3-d block added to the User Data array in Figure 8.

35 U.S.C. 103(a) rejection of claim 17.

Figure 13A in Rhines teaches the first set of encoded data is stored in a row encode storage array, wherein the row encode storage array includes a plurality of row array bits.

35 U.S.C. 103(a) rejection of claim 18.

Rhines substantially teaches the claimed invention described in claims 1-3 (as rejected above).

However Rhines does not explicitly teach the specific use of resetting the row encode storage array such that all row array bits are set to zero, wherein the step of resetting is executed after the first set of encoded data is outputted.

The Examiner asserts that the values of the C2 parity bits of Figures 4A, 4B and 5 in Rhines does not matter since any previous values would be discarded and replaced with newly calculated C2 parity bits because the current C2 parity bits only depend on the current calculation.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Rhines by including use of resetting the row encode storage array such that all row array bits are set to zero after the first set of encoded data is outputted and before the step of performing the parity calculation along

Art Unit: 2133

the hyper diagonal is executed. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of resetting the row encode storage array such that all row array bits are set to zero after the first set of encoded data is outputted and before the step of performing the parity calculation along the hyper diagonal is executed would not have mattered since any previous values would be discarded and replaced with newly calculated C2 parity bits because the current C2 parity bits only depend on the current calculation.

35 U.S.C. 103(a) rejection of claim 19.

Figure 13A in Rhines teaches the first set of encoded data is stored in a row encode storage array, wherein the row encode storage array includes a plurality of row array bits.

35 U.S.C. 103(a) rejection of claim 20.

Figure 4B in Rhines teaches the hyper set of encoded data is stored in a hyper parity array, wherein the hyper parity array includes a plurality of parity array bits.

35 U.S.C. 103(a) rejection of claim 21.

Col. 4, lines 59-62 and col. 10, lines 31-68 in Rhines teach that prior to generating the C2 error correction 90 of Figure 2 in Rhines, the rows of the first series of data planes 40, 42 and 44 in Figures 4A and 5 are orthogonally shuffled by the outer Interleaver 16

Art Unit: 2133

so that the new block of Figure 4B is formed whereby the x-y planes of the new block of Figure 4B are the diagonal planes of the Block in Figure 4A, hence the column encoding of the new block of Figure 4B to from the C2 error correction of Figures 2 and 8 is equivalent and is a means for performing a parity calculation along a hyper diagonal in the Block in Figure 4A, wherein a parity result for the C2 parity calculation of Figure 8 is generated; Note: the Middle C2 encoder must iteratively receive user data information bits in hyper columns since Middle C2 hyper column encoder 90 in Figure 2 is a hyper column encoder.

35 U.S.C. 103(a) rejection of claim 22.

Rhines substantially teaches the claimed invention described in claims 1-3 (as rejected above).

However Rhines does not explicitly teach the specific use of initializing the parity array such that the parity bits are set to zero before the step of performing the parity calculation along the hyper diagonal is executed.

The Examiner asserts that the values of the C2 parity bits of Figures 4A, 4B and 5 in Rhines does not matter since any previous values would be discarded and replaced with newly calculated C2 parity bits because the current C2 parity bits only depend on the current calculation.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Rhines by including use of initializing the parity array such that the parity bits are set to zero before the step of performing the

Art Unit: 2133

parity calculation along the hyper diagonal is executed. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of initializing the parity array such that the parity bits are set to zero before the step of performing the parity calculation along the hyper diagonal is executed would not have mattered since any previous values would be discarded and replaced with newly calculated C2 parity bits because the current C2 parity bits only depend on the current calculation.

35 U.S.C. 103(a) rejection of claim 31.

The shuffling steps of Figures 4A, 4B and 5 in Rhines are a means for rotating the parity array for calculating C2 parity such that the C2 parity result stored in the C2 parity array is substantially aligned with the hyper diagonal planes in Figure 4B along which the C2 parity result was calculated.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number

for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2133

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business

Cepter (EBC) (4/866-217-9197 (toll-free).

Joseph D/Tdrres, J Art Unit 2/133